UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,310	11/23/2004	Roman Woyzichovski	10901/81	6114

26646 7590 09/05/2008

KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER	
PERILLA, JASON M	
ART UNIT	PAPER NUMBER
2611	
MAIL DATE	DELIVERY MODE
09/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/501,310	WOYZICHOVSKI, ROMAN	
	Examiner	Art Unit	
	JASON M. PERILLA	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 21-42 are pending in the instant application.

Response to Amendment/Argument

2. The Applicant's remarks, filed June 2, 2008, have been considered by the Examiner.

The Applicant's remarks regarding the rejection of claim 29 under 35 U.S.C. § 112, second paragraph, are not persuasive. The claims provide that "the low value part" (which corresponds to least significant bits of the address bits) corresponds to a fractional proportion *of the address values*. However, by the Applicant's own reference to the specification, it is clear that the low value part of the address sequence corresponds to a fractional proportion *of a phase value*. The present claims fail to even embody the invention and are indefinite because one is unable to determine a fraction of address values of an address bit sequence. Claim 28 should also be reconsidered by the Applicant.

The Applicant has presented the following arguments against the Liessner (U.S. Pat. No. 5079549) in view of Garverick et al (U.S. Pat. No. 5134578; "Garverick") prior art combination's application to the claims: (1) the combination does not support a fully digital implementation of the claimed invention and requires a substantial redesign of the primary reference Liessner, (2) Liessner does not disclose generating new correctional values in accordance with a quality criterion, and (3) Liessner does not disclose accumulating results for generating correctional values over a specifiable time interval.

Regarding the Applicant's argument (1), as applied in the combination of Liessner in view of Garverick presented in the previous office actions and below, the combination results in a digital implementation of many of Liessner's original analog components. The Applicant's suggestion that such a "redesign" from an analog to a digital embodiment would "change the basic principal under which the device described by Liessner was designed to operate" (6/2/08 remarks, pg. 9) is not persuasive. Rather, Liessner's "basic principal" of operation would be maintained in a fully digital implementation as would be readily understood by one having ordinary skill in the art. As is notoriously known and understood in the art, properly designed digital implementations provide for zero loss in signal integrity as compared to analog ones. Moreover, the conversion of Liessner's analog components to digital ones would involve merely a routine level of skill in the art and would produce only expected and predictable results.

Regarding the Applicant's argument (2), as broadly as claimed, Liessner does disclose generating new correctional values in accordance with a quality criterion. The new correction values (i.e. Liessner fig. 1, outputs of refs. 16 and 18 as updated by feedback) are generated in accordance with the use of a "dead zone" (see fig. 3) which "prevents spurious triggering" (col. 3, lines 60-65). The dead zone which prevents spurious triggering is applied as "the quality criterion". Namely, "the quality criterion" requires that the error signal ES must be of sufficient amplitude (col. 3, lines 50-60) to produce UP or DOWN outputs (i.e. fig. 4A, UP or DOWN) for accumulation.

Regarding the Applicant's argument (3), the accumulation of UP and DOWN outputs (via fig. 4A, refs. 25 and 27) from Liessner's the error signal detector (fig. 4A, ref. 22) is performed over a specifiable time interval because it is limited by the disable pulse generator (fig. 4A, ref. 29). As broadly as claimed, even if the disable pulse generator 29 merely prevents the outputs of the UP (25) and DOWN (27) count generators from being updated to the SIN and COS lookup tables, it yet causes their respective accumulation outputs "UP COUNT" and "DOWN COUNT" to be "specifiable" as claimed. Therefore, their "accumulations" are specifiable.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 29 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 29, the claim is rejected because one skilled in the art is unable to determine a definite meaning for a "fractional proportion" of an address sequence. As commonly understood in the art, an address sequence consists of a number of address bits. The claim is indefinite because one is unable to determine how a fraction of a bit may be determined. Moreover, the Examiner suggests that the terms "high-value" and "low-value" are replaced with the more accepted language of "most-significant" and "least-significant" with respect to the address bits.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 21-24, 26, 27, and 30-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner (U.S. Pat. No. 5079549 – previously cited) in view of Garverick et al (U.S. Pat. No. 5134578; "Garverick" – previously cited).

Regarding claim 21, Liessner discloses a method for interpolating (col. 2, lines 20-25) at least two position-dependent, periodic analog signals (fig. 1, SIN(X), COS(X)) that are phase-shifted with respect to one another and which are generated by scanning a measuring scale (abstract), comprising: generating a string of results (fig. 1, "ERROR SIGNAL") by combining (fig. 1, ref. 20) the periodic analog signals with correctional values (fig. 1, outputs of 16 and 18) and subsequently combining the periodic analog signals with one another; generating from the string of results (a) new correctional values (new or updated outputs of fig. 1, refs. 16 and 18) in accordance in accordance with a quality criterion (fig. 1, output of error "DETECTOR"; "ES>0" or "ES<0") that is to be satisfied during interpolation (col. 3, lines 40-55) and (b) output signals of the interpolation (fig. 1, "Y"); accumulating (fig. 1, ref. 24; fig. 4A, refs. 25 and 27) over a specifiable time interval (according to disable pulse generator, i.e. fig. 4A, ref. 29) values of the combination output for generating the correctional values (outputs of fig. 1, refs. 16 and 18) and output signals (fig. 1, "Y"); and using a signal sequence

generated by the accumulation as an address sequence (also fig. 1, “Y”) for generating the correctional values and for generating the output signals (fig. 1). Liessner discloses that the multipliers or combiners (fig. 1, refs. 12 and 14) which combine the periodic analog signals (fig. 1, SIN(X), COS(X)) with correctional values (fig. 1, outputs of 16 and 18) are “multiplying digital to analog converters that cause a digital input to attenuate an analog signal” (col. 3, lines 25-30). Therefore, the outputs from the lookup tables (fig. 1, refs. 16 and 18) are digital and the periodic signals (fig. 1, SIN(X), COS(X)) are analog ones which are attenuated according to the outputs from the lookup tables. Liessner does not explicitly disclose using sigma-delta modulators to convert the periodic analog signals into digital signals. However, the use of digital data to represent analog waveforms is notoriously known in the art as evidenced by Garverick. The use of sigma-delta analog to digital converters is notoriously known in the art as evidenced by Garverick. Garcerick discloses the use of several sigma-delta analog to digital converters (fig. 1, refs. 21-26) to convert various phases of an analog signal into digital form (col. 4, lines 14-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the Liessner’s "rotary or linear encoder” output (fig. 1, "SIN(X)" and "COS(X)") could be converted into digital form before being fed to multipliers (fig. 1, refs. 12 and 14) as suggested by Garverick. In the combination of Liessner in view of Garverick, Liessner’s embodiment must be converted to a purely digital one. One skilled in the art would be enabled to complete the conversion with

knowledge readily known in the art and motivated to complete the conversion because of the advantages provided by digital implementations of analog devices. Namely, proper digital implementations provide for zero loss in signal integrity as notoriously understood in the art.

Regarding claims 22 and 23, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, as broadly as claimed, Liessner's counter (fig. 1, ref. 24) is considered to be both a filter and an integrator because its output depends upon an accumulation of the past inputs.

Regarding claim 24, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses forming the address sequence (fig. 1, "Y") from the accumulation (fig. 1, ref. 24), the address sequence including address values that represent phase information of the analog signals (col. 3, lines 35-40).

Regarding claim 26, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses that the address values are a linear function of the phases of the periodic signals when the quality criterion is satisfied. The address values are a linear function of the phases because the error of phases directly determine the address values in a linear fashion (col. 4, lines 19-38).

Regarding claim 27, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses that the address

sequence (fig. 1, "Y") represent a phase value having a fractional proportion (col. 3, lines 35-40).

Regarding claim 30, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the generation of new correctional values is in accordance with the quality criterion (amount of error) until it is satisfied because the embodiment is a closed loop embodiment (fig. 1).

Regarding claim 31, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses storing possible correction values as predefined values in an assignment unit (col. 3, lines 35-40).

Regarding claim 32, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses the remaining limitations of the claim as applied in claim 21 above.

Regarding claim 33, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the correctional values correspond to values of a trigonometric function (col. 3, lines 35-40).

Regarding claim 34, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the analog signals are phase shifted by 90 degrees with respect to each other as applied in claim 21 above.

Regarding claim 35, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the analog signals are substantially sinusoid as applied in claim 21 above.

Regarding claim 36, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses the remaining limitations of the claim as applied to claim 21 above. Liessner discloses adding (fig. 1, ref. 20) subsequent to multiplying (fig. 1, refs. 12 and 14).

Regarding claim 37, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, it is inherent that a piece of data may have a word width of one bit as understood by one having ordinary skill in the art.

Regarding claim 38, Liessner in view of Garverick disclose the limitations of claim 36 as applied above. Further, Liessner discloses the remaining limitations of the claim as applied to claim 21 above. Liessner discloses adding (fig. 1, ref. 20) subsequent to reducing or attenuating (fig. 1, refs. 12 and 14; col. 3, lines 25-30; “attenuating”).

Regarding claim 39, Liessner in view of Garverick disclose the limitations of claim 38 as applied above. Further, Liessner discloses combining by addition (fig. 1, ref. 20) the correctional values. Furthermore, in the purely digital implementation of Liessner in view of Garverick, the addition of the correctional values would result in one of four possibilities as understood by one having ordinary skill in the art because no other possibilities could exist.

Regarding claim 40, Liessner in view of Garverick disclose the limitations of the claim as applied to claim 21 above.

Regarding claim 41, Liessner in view of Garverick disclose the limitations of the claim as applied to claim 21 above.

Regarding claim 42, Liessner in view of Garverick disclose the limitations of the claim as applied to claim 21 above. Liessner in view of Garverick do not explicitly disclose an evaluation circuit post-connected to the filter configured to convert address values of the address sequence into output values of the interpolation. However, Liessner discloses that “the digital output signal y is provided that *represents* displacement within a reticle cycle" (col. 2, lines 25-30). Because the digital output signal y only “represents” the displacement, it is obvious to one having ordinary skill in the art that an evaluation circuit would be required to convert the digital address value y into more useful information. Moreover, Liessner suggests that the evaluation circuit may be a memory lookup table such as references 16 or 18 of figure 1 (col. 3, lines 35-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that an evaluation unit would be required to convert Liessner’s y address values into a more useable format for their utility.

7. Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner in view of Garverick, and in further view of The Applicant’s Admitted Prior Art (“AAPA”).

Regarding claim 25, Liessner in view of Garverick disclose the limitations of claim 24 as applied above. Liessner does not explicitly disclose that the output signals (fig. 1, "Y") are generated from the address sequence by low- pass filtering and assignment of the address values. However, low-pass filtering and assignment of the address values is well known in the art as evidenced in the discussion of the AAPA (page 2, lines 7-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the address sequence of Liessner could be fed through a low-pass filter (i.e. within UP/DOWN counter 26 of figure 1) as suggested by the AAPA because it was a well known method in the art.

8. Claims 28 and 29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner in view of Garverick, and Khan et al (U.S. Pat. Pub. 2002/0116181; hereafter "Khan" – newly cited).

Regarding claim 28, Liessner in view of Garverick disclose the limitations of claim 27 as applied above. Liessner in view of Garverick do not explicitly disclose that the correctional values are generated in the correctional value generating step in accordance with a high-value part and low-value part of the address sequence, the high-value part corresponding to an integer portion of the address values. However, Khan teaches an exemplary sine/cosine mapper according to figure 2 for determining from an upper two bits (input to 222) of the phase accumulation a quadrant in which a phase corresponding to the phase accumulation is located on an X-Y coordinate plane (para. 0055), a look-up table

(226) for storing a predetermined number of sine or cosine values for one of four determined quadrants of the X-Y coordinate plane, and outputting a sine or cosine value (20 bits each "COS" and "SIN" output from 226) according to bits of the phase accumulation other than the upper two bits (i.e. “lower bits”; 18 remaining bits of 20 not fed into "OUTPUT SELECT" 222), and a cosine and sine value calculator (222) for calculating the sine and cosine values having phase corresponding to the phase accumulation according to the determined quadrant and the sine or cosine value received from the look-up table (paras. 0055-0058). Khan teaches the implementation of the mapper is effective and reduces overhead (para. 0010). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the sine/cosine lookup tables of Liessner (fig. 1, refs. 12 and 14) could be replaced by the implementation taught by Khan because it is an effective method which reduces overhead.

Regarding claim 29, Liessner in view of Garverick disclose the limitations of claim 27 as applied above. Further, Liessner in view of Garverick, and Khan disclose the remaining limitations of the claim as applied to claim 28 above.

Allowable Subject Matter

9. No claims are allowed.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M Perilla/
Art Unit 2611
August 21, 2008

/jmp/

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611